GS1575A / GS9075A HD-LINX® II Multi-Rate SDI Automatic Reclocker

Features

GS1575A

- SMPTE 292M, 259M and 344M compliant
- Supports data rates of 143, 177, 270, 360, 540, 1483.5, 1485 Mb/s
- Supports DVB-ASI at 270Mb/s
- Pb-free and RoHS Compliant
- Auto and Manual Modes for rate selection
- Standards indication in Auto Mode
- 4:1 input multiplexer
- Loss of Signal (LOS) Output
- Lock Detect Output
- On-chip Input and Output Termination
- Differential 50Ω inputs and outputs
- Mute, Bypass and Autobypass functions
- SD/HD indication output to control GS1528A Dual Slew-Rate Cable Driver
- Single 3.3V power supply
- Operating temperature range: 0°C to 70°C

GS9075A

- SMPTE 259M and 344M compliant
- Supports data rates of 143, 177, 270, 360, and 540Mb/s
- Supports DVB-ASI at 270Mb/s
- Pb-free and RoHS Compliant
- Auto and Manual Modes for rate selection
- Standards indication in Auto Mode
- 4:1 input multiplexer
- Loss of Signal (LOS) Output
- Lock Detect Output
- On-chip Input and Output Termination
- Differential 50Ω inputs and outputs
- Mute, Bypass and Autobypass functions
- Single 3.3V power supply
- Operating temperature range: 0°C to 70°C

Applications

GS1575A

- SMPTE 292M, SMPTE 259M and SMPTE 344M Serial Digital Interfaces

GS9075A

- SMPTE 259M and SMPTE 344M Serial Digital Interfaces.

Description

The GS1575A/9075A is a Multi-Rate Serial Digital Reclocker designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data.

The GS1575A Serial Digital Reclocker will recover the embedded clock signal and re-time the data from a SMPTE 292M, SMPTE 259M or SMPTE 344M compliant digital video signal.

The GS9075A Serial Digital Reclocker will recover the embedded clock signal and re-time the data from a SMPTE 259M or SMPTE 344M compliant digital video signal.

The GS1575A/9075A removes the high frequency jitter components from the bit-serial stream. Input termination is on-chip for seamless matching to 50Ω transmission lines. An LVPECL compliant output interfaces seamlessly to the GS1578A/GS9078A Cable Driver.

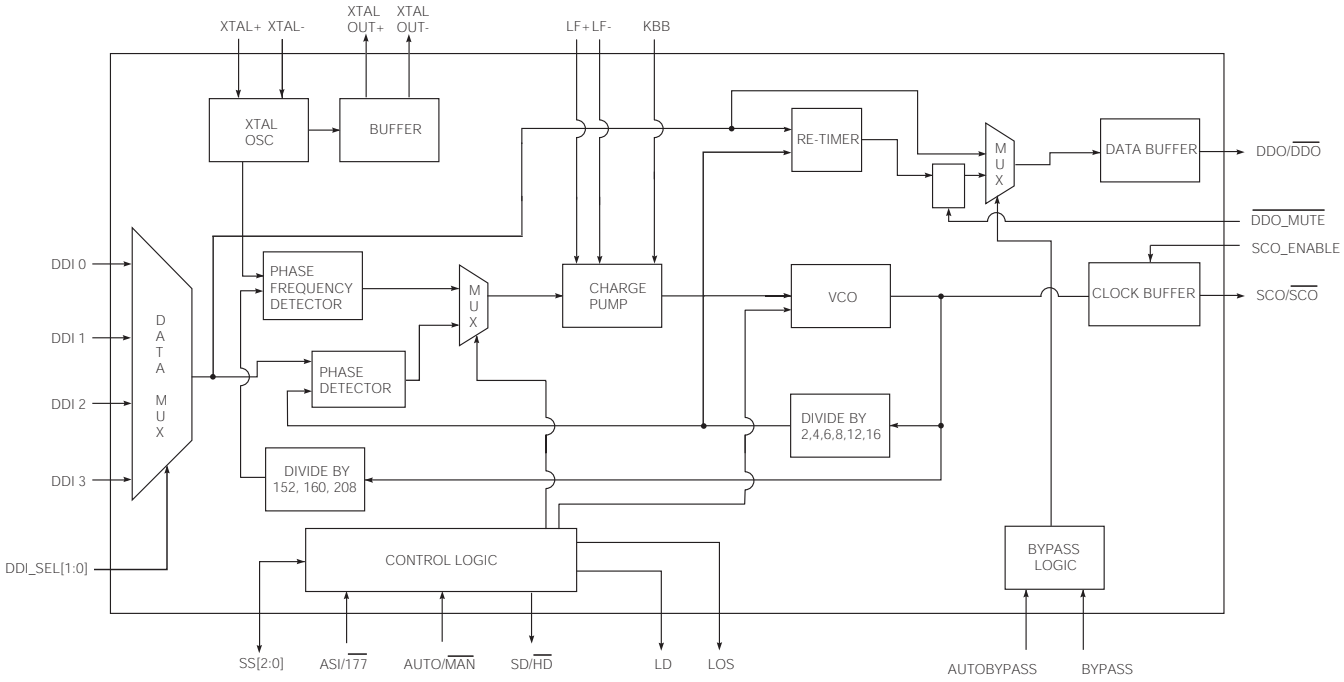
The GS1575A/9075A can operate in either auto or manual rate selection mode. In Auto mode the device will automatically detect and lock onto incoming SMPTE SDI data signals at any supported rate. For single rate data systems, the GS1575A/9075A can be configured to operate in Manual mode. In both modes, the device requires only one external crystal to set the VCO frequency when not locked and provides adjustment free operation.

In systems which require passing of non-SMPTE data rates, the GS1575A/9075A can be configured to either automatically or manually enter a bypass mode in order to pass the signal without reclocking.

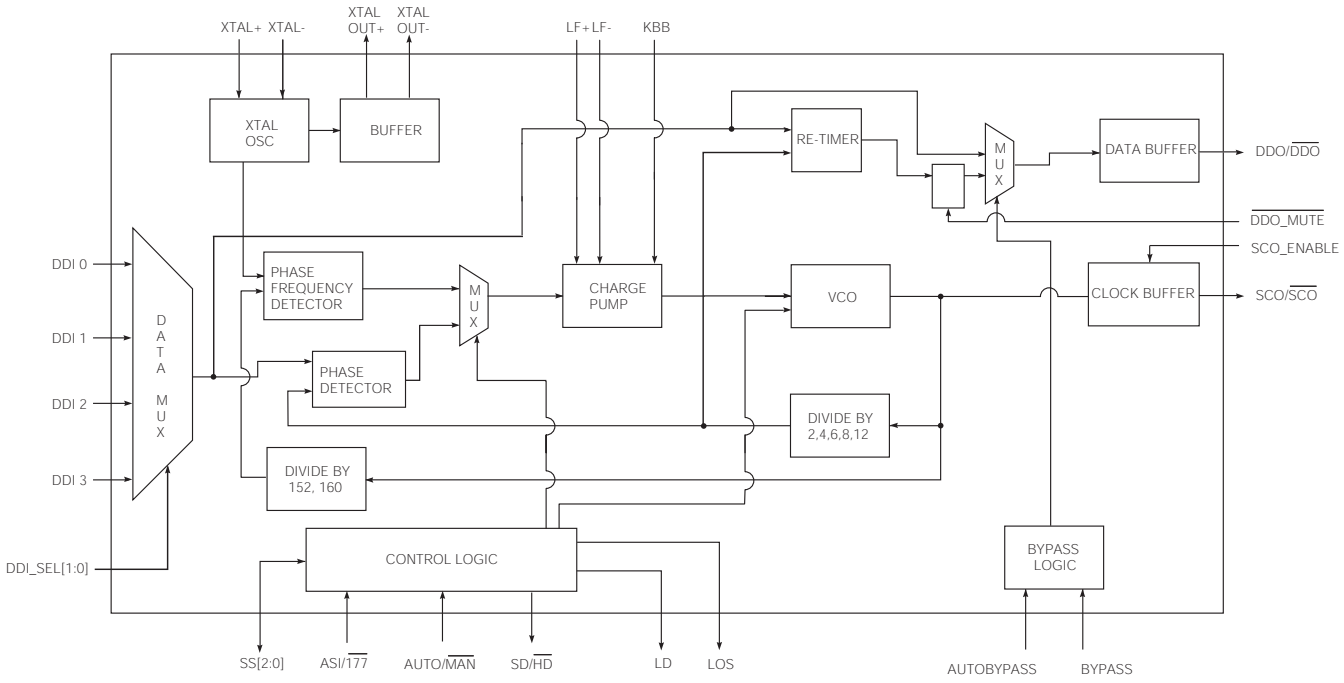
The ASI/$\overline{177}$ input pin allows for manual selection of support of either 177Mb/s or DVB-ASI inputs.

The GS1575A/9075A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous sub-components are RoHS compliant.



GS1575A Functional Block Diagram



GS9075A Functional Block Diagram

Contents

1. Pin Out

1.1 GS1575A Pin Assignment

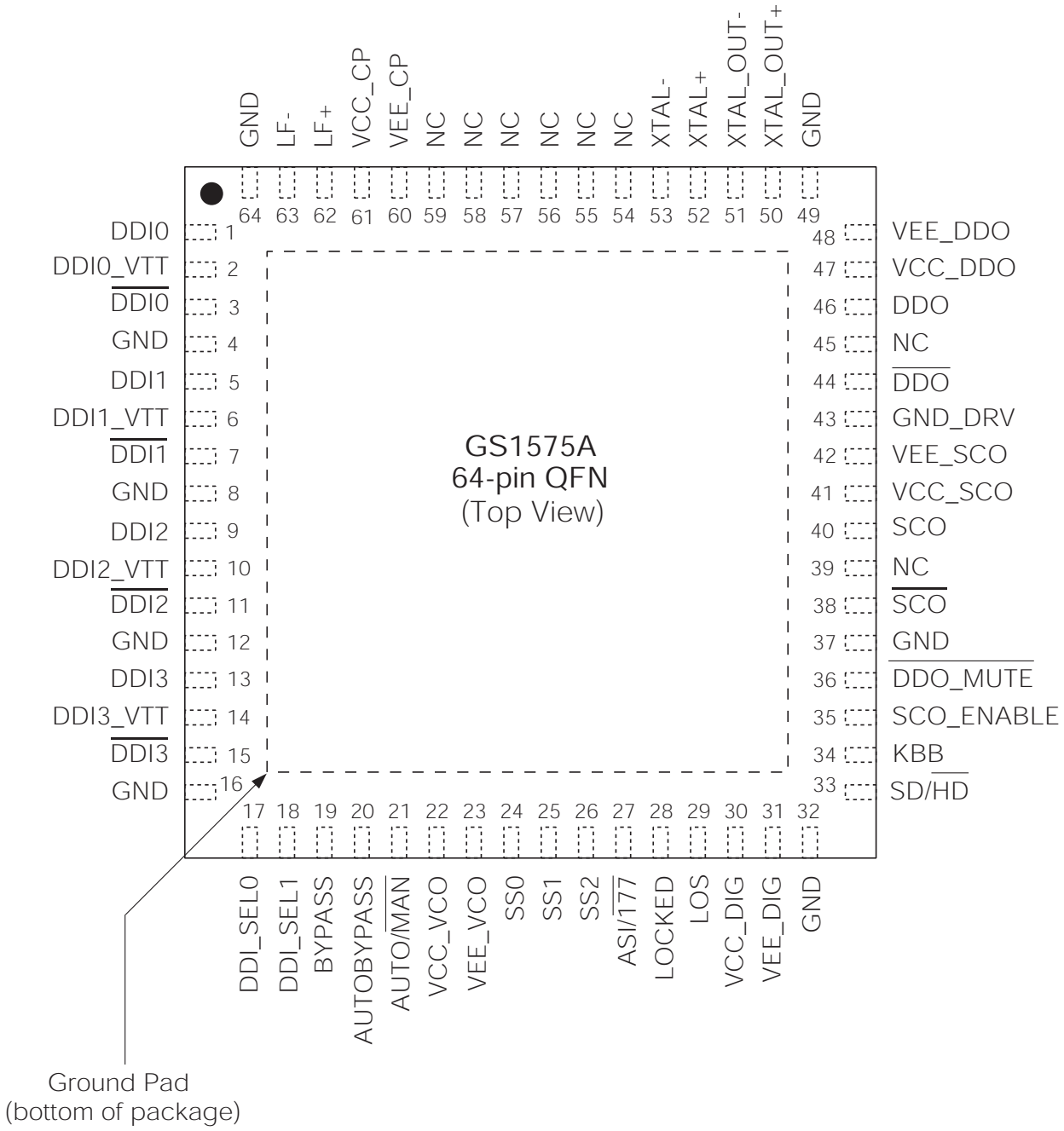


Figure 1-1: 64-Pin QFN

1.2 GS9075A Pin Assignment

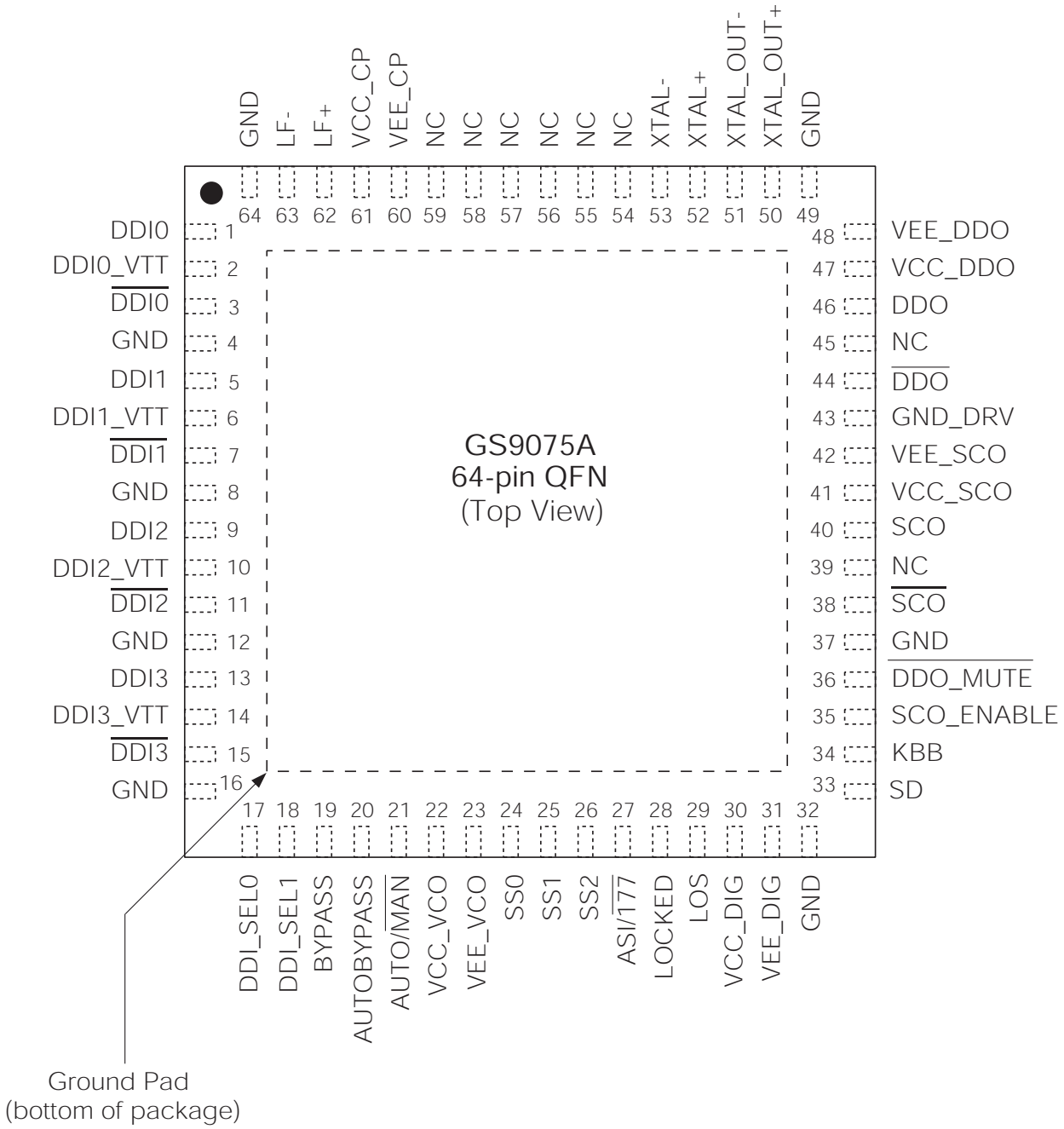


Figure 1-2: 64-Pin QFN

1.3 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 3	DDI0, $\overline{\text{DDI0}}$	Input	Serial digital differential input 0.
2	DDI0_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI0 and $\overline{\text{DDI0}}$.
4, 8, 12,16, 32, 37, 43, 49, 64	GND	Passive	Recommended connect to GND.
5, 7	DDI1,$\overline{\text{DDI1}}$	Input	Serial digital differential input 1.
6	DDI1_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI1 and $\overline{\text{DDI1}}$.
9, 11	DDI2, $\overline{\text{DDI2}}$	Input	Serial digital differential input 2.
10	DDI2_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI2 and $\overline{\text{DDI2}}$.
13, 15	DDI3, $\overline{\text{DDI3}}$	Input	Serial digital differential input 3.
14	DDI3_VTT	Passive	Center tap of two 50Ω on-chip termination resistors between DDI3 and $\overline{\text{DDI3}}$.
17, 18	DDI_SEL[1:0]	Logic Input	Serial digital input select.
19	BYPASS	Logic Input	Bypass the reclocker stage. When BYPASS is HIGH, it overwrites the AUTOBYPASS setting.
20	AUTOBYPASS	Logic Input	Automatically bypasses the reclocker stage when the PLL is not locked This pin is ignored when BYPASS is HIGH.
21	AUTO/$\overline{\text{MAN}}$	Logic Input	Auto/Manual select. When set HIGH, the standard is automatically detected from the input data rate. When set LOW, the user must program the input standard using the SS[2:0] pins.
22	VCC_VCO	Power	Most positive power supply connection for the internal VCO section. Connect to 3.3V.
23	VEE_VCO	Power	Most negative power supply connection for the internal VCO section. Connect to GND.

DDI_SEL1	DDI_SEL0	INPUT SELECTED
0	0	DDI0
0	1	DDI1
1	0	DDI2
1	1	DDI3

Table 1-1: Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>24, 25, 26</td><td>SS[2:0]</td><td>Bi-directional</td><td>When AUTO/$\overline{\text{MAN}}$ is HIGH, SS[0:2] are outputs, displaying the data rate to which the PLL has locked.
When AUTO/$\overline{\text{MAN}}$ is LOW, SS[0:2] are inputs, forcing the PLL to lock only to a selected data rate
<table>
<tr><th>SS2</th><th>SS1</th><th>SS0</th><th>DATA RATE SELECTED/FORCED (Mb/s)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>143</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>177</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>270</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>360</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>540</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1483.5/1485</td></tr>
</table></td></tr>
<tr><td>27</td><td>ASI/$\overline{177}$</td><td>Logic Input</td><td>When set HIGH, the device disables the 177Mb/s data rate in the data rate detection circuit. This prevents a false lock to 177Mb/s when using DVB-ASI.
When set LOW, 177Mb/s lock is possible, however, if a 270Mb/s ASI signal is applied, the device could false lock to the 177MHz signal.</td></tr>
<tr><td>28</td><td>LOCKED</td><td>Output</td><td>Lock Detect.
This pin is set HIGH by the device when the PLL is locked.</td></tr>
<tr><td>29</td><td>LOS</td><td>Output</td><td>Loss of Signal.
Set HIGH when there are no transitions on the active DDI[3:0] input. See Lock and LOS Indicators on page 21.</td></tr>
<tr><td>30</td><td>VCC_DIG</td><td>Power</td><td>Most positive power supply connection for the internal glue logic.
Connect to 3.3V.</td></tr>
<tr><td>31</td><td>VEE_DIG</td><td>Power</td><td>Most negative power supply connection for the internal glue logic.
Connect to GND.</td></tr>
<tr><td>33</td><td>SD/$\overline{\text{HD}}$
(GS1575A only)</td><td>Output</td><td>This signal will be set LOW by the device when the reclocker has locked to 1.485Gbps or 1.485/1.001Gbps, or when a non-SMPTE standard is applied (i.e. the device is not locked).
It will be set HIGH when the reclocker has locked to 143Mbps, 177Mbps, 270Mbps, 360Mbps, or 540Mbps.</td></tr>
<tr><td>33</td><td>SD
(GS9075A only)</td><td>Output</td><td>This signal will go HIGH when the reclocker has locked to the input SD signal. It will be LOW otherwise.</td></tr>
<tr><td>34</td><td>KBB</td><td>Analog Input</td><td>Controls the loop bandwidth of the PLL.
Leave this pin floating for serial reclocking applications.</td></tr>
<tr><td>35</td><td>SCO_ENABLE</td><td>Power</td><td>Serial clock output enable.
Connect to VCC to enable the serial clock output. Connect to GND to disable the serial clock output.
NOTE: This is not a TTL signal input.</td></tr>
</table>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
36	$\overline{\text{DDO\_MUTE}}$	Logic Input	Mutes the DDO/$\overline{\text{DDO}}$ outputs. This option is not available in bypass mode.
38, 40	$\overline{\text{SCO}}$, SCO	Output	Serial clock output. When SCO_ENABLE is set HIGH, a serial digital differential clock will be presented to the application layer at the selected data rate.
39, 45, 54 - 59	NC	No Connect	Not connected internally.
41	VCC_SCO	Power	Most positive power supply connection for the SCO/$\overline{\text{SCO}}$ output driver. Connect to 3.3V.
42	VEE_SCO	Power	Most negative power supply connection for the SCO/$\overline{\text{SCO}}$ output driver. Connect to GND.
43	GND_DRV	Passive	Recommended connect to GND.
44, 46	$\overline{\text{DDO}}$, DDO	Output	Differential Serial Digital Outputs.
47	VCC_DDO	Power	Most positive power supply connection for the DDO/$\overline{\text{DDO}}$ output driver. Connect to 3.3V.
48	VEE_DDO	Power	Most negative power supply connection for the DDO/$\overline{\text{DDO}}$ output driver. Connect to GND.
50, 51	XTAL_OUT+, XTAL_OUT-	Output	Differential outputs of the reference oscillator used for monitoring or test purposes.
52, 53	XTAL+, XTAL-	Input	Reference crystal input. Connect to the GO1535 as shown in the Typical Application Circuits on page 23.
60	VEE_CP	Power	Most negative power supply connection for the internal charge pump. Connect to GND.
61	VCC_CP	Power	Most positive power supply connection for the internal charge pump. Connect to 3.3V.
62, 63	LF+, LF-	Passive	Loop filter capacitor connection. Connect as shown in the Typical Application Circuits on page 23.
–	Center Pad	–	Ground pad on bottom of package. Solder to main ground plane following recommendations under Recommended PCB Footprint on page 26.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	+3.6 V_{DC}
Input Voltage	Vcc + 0.5V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-50°C < T_s < 125°C
Input ESD Voltage	1kV
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	Operating Range	3.135	3.3	3.465	V
Supply Current	I_{CC}	SCO enabled, T_A=25°C	–	215	260	mA
	I_{CC}	SCO disabled, T_A=25°C	–	195	230	mA
Power Consumption	–	SCO enabled, T_A=25°C	–	710	–	mW
	–	SCO disabled, T_A=25°C	–	645	–	mW
Logic Inputs DDI_SEL[1:0], BYPASS, $\overline{\text{AUTOBYPASS}}$, AUTO/$\overline{\text{MAN}}$, ASI/$\overline{177}$, $\overline{\text{DDO\_MUTE}}$	V_{IH}	High	2.0	–	–	V
	V_{IL}	Low	–	–	0.8	V
Logic Outputs SD/$\overline{\text{HD}}$, LOCKED, LOS	V_{OH}	250uA Load	2.8	–	–	V
	V_{OL}	250uA Load	–	–	0.5	V
Bi-Directional Pins (Manual Mode) SS[2:0], AUTO/$\overline{\text{MAN}}$ = 0	V_{IH}	High	2.0	–	–	V
	V_{IL}	Low	–	–	0.8	V

Table 2-1: DC Electrical Characteristics (Continued)

V_{CC} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Bi-Directional Pins (Auto Mode) SS[2:0], AUTO/$\overline{MAN}$ = 1	V_{OH}	High, 250uA Load	2.8	–	–	V
	V_{OL}	Low, 250uA Load	–	–	0.5	V
XTAL_OUT+, XTAL_OUT-	V_{OH}	High	–	V_{CC}	–	V
	V_{OL}	Low	–	V_{CC} - 0.285	–	V
SCO_ENABLE	–	1.5mA of current delivered	V_{CC} - 0.165	–	V_{CC} + 0.165	V
Serial Input Voltage	–	Common Mode	1.65 + (V_{SID}/2)	–	V_{CC} - (V_{SID}/2)	V
Serial Output Voltage SDO/$\overline{SDO}$, SCO/$\overline{SCO}$	–	Common Mode	–	V_{CC} - (V_{OD}/2)	–	V

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Input Data Rate	–	GS1575A	143	–	1485	Mb/s
	–	GS9075A	143	–	540	Mb/s
Serial Input Jitter Tolerance	–	Worst case modulation (e.g. square wave modulation) 143, 270, 360, 1485 Mb/s	0.8	–	–	UI
PLL Lock Time - Asynchronous	t_{ALOCK}	–	–	–	10	ms
PLL Lock Time - Synchronous	t_{SLOCK}	C_{LF}=47nF, SD/$\overline{HD}$=0	–	–	10	us
	t_{SLOCK}	C_{LF}=47nF, SD/$\overline{HD}$=1	–	–	39	us
Serial Output Rise/Fall Time SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$ (20% - 80%)	t_{rSDO},t_{rSCO}	50Ω load (on chip)	–	114	–	ps
	t_{fSDO},t_{fSCO}	50Ω load (on chip)	–	106	–	ps
Serial Digital Input Signal Swing	V_{SID}	Differential with internal 100Ω input termination See Figure 2-1	100	–	800	mV_{p-p}
Serial Digital Output Signal Swing SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$	V_{OD}	100Ω load differential See Figure 2-2	1400	1600	2200	mV_{p-p}

Table 2-2: AC Electrical Characteristics (Continued)

V_{CC} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Jitter SDO/$\overline{SDO}$ and SCO/$\overline{SCO}$ KBB = Float PRN, 2^{23}-1 Measurement is output jitter that includes input jitter from BERT.	t_{OJ}	143 Mb/s	–	0.02	–	UI
	t_{OJ}	177 Mb/s	–	0.02	–	UI
	t_{OJ}	270 Mb/s	–	0.02	0.09	UI
	t_{OJ}	360 Mb/s	–	0.03	–	UI
	t_{OJ}	540 Mb/s	–	0.03	0.09	UI
	t_{OJ}	1485 Mb/s (GS1575A only)	–	0.06	0.13	UI
	t_{OJ}	Bypass	–	0.06	0.13	UI
Loop Bandwidth	BW_{LOOP}	1.485 Gb/s, KBB = FLOAT (GS1575A only)	–	1.75	–	MHz
	BW_{LOOP}	1.485 Gb/s, KBB = GND, <0.1dB Peaking (GS1575A only)	–	3.2	–	MHz
	BW_{LOOP}	270 Mb/s, KBB = FLOAT	–	520	–	KHz
	BW_{LOOP}	270 Mb/s, KBB = GND	–	1000	–	KHz

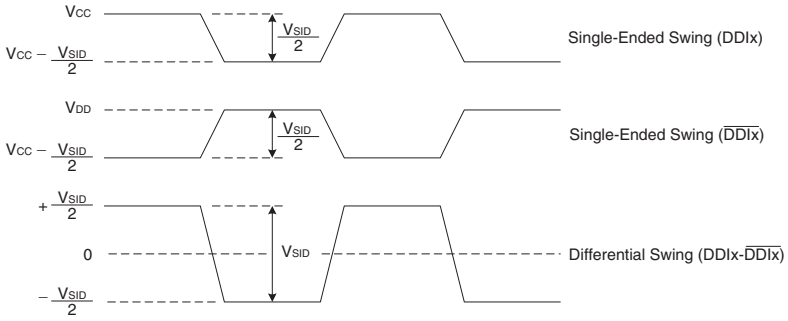


Figure 2-1: Serial Digital Input Signal Swing

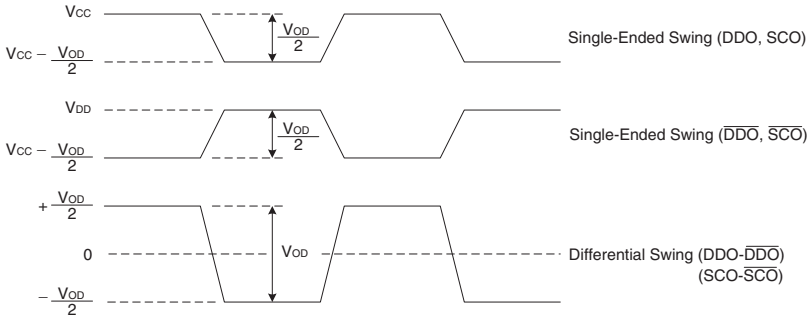


Figure 2-2: Serial Digital Output Signal Swing

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-3. The recommended standard Pb reflow profile is shown in Figure 2-4.

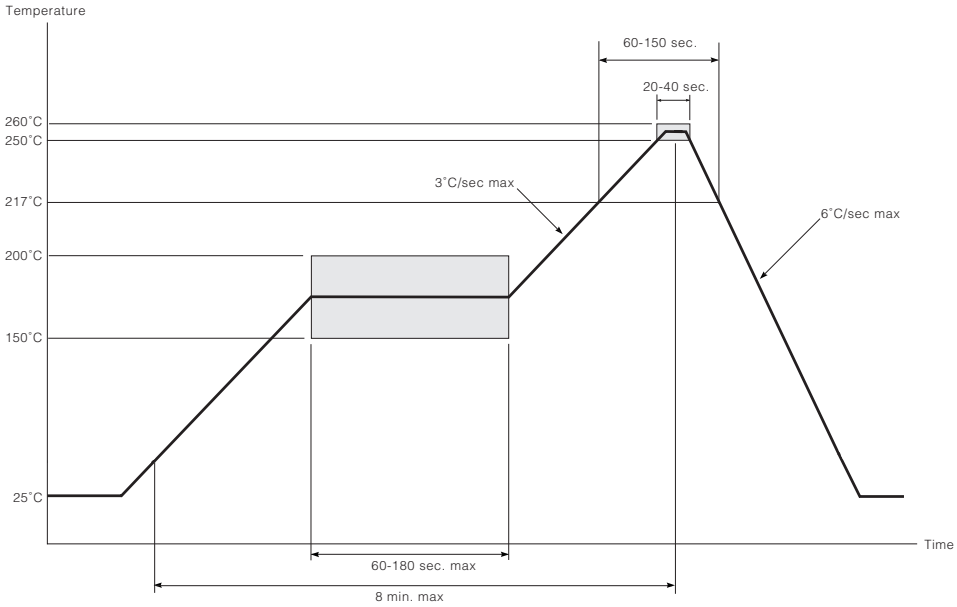


Figure 2-3: Maximum Pb-free Solder Reflow Profile (Preferred)

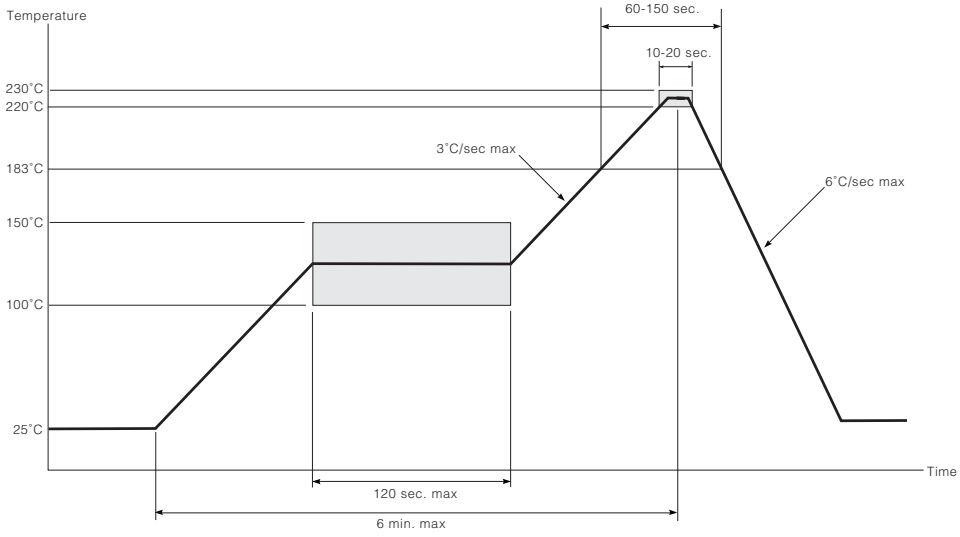


Figure 2-4: Standard Pb Solder Reflow Profile (Pb-free package)

3. Input / Output Circuits

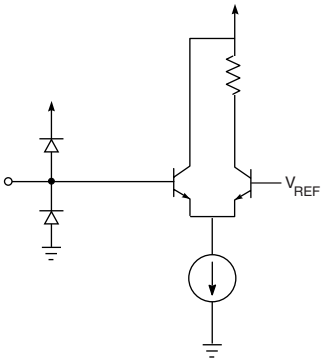


Figure 3-1: TTL Inputs

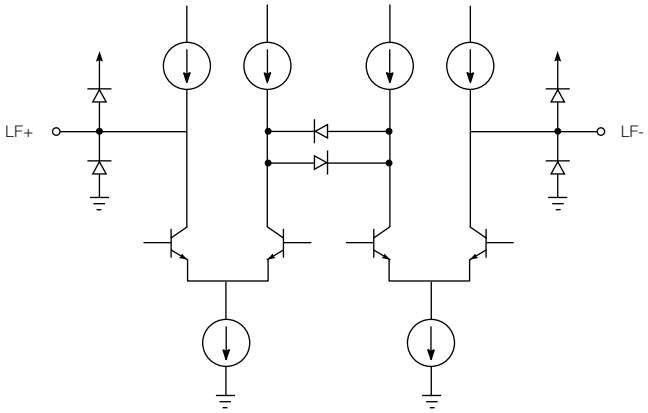


Figure 3-2: Loop Filter

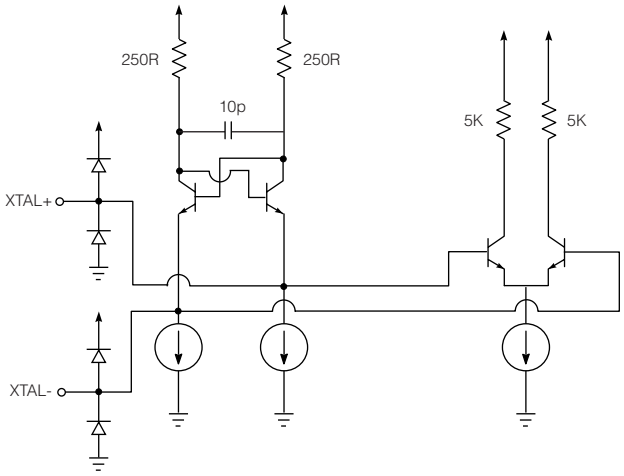


Figure 3-3: Crystal Input

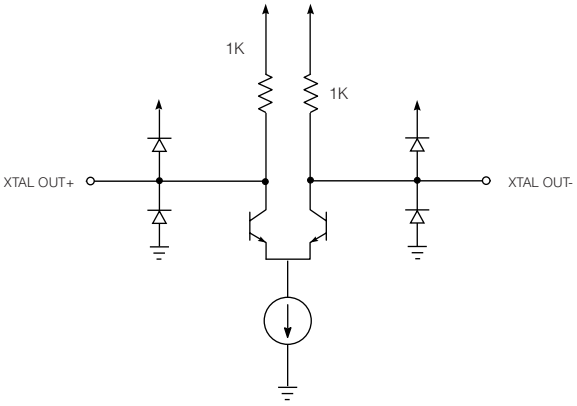


Figure 3-4: Crystal Output Buffer

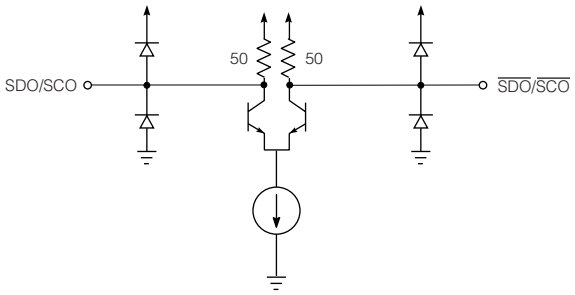


Figure 3-5: Serial Data Outputs, Serial Clock Outputs

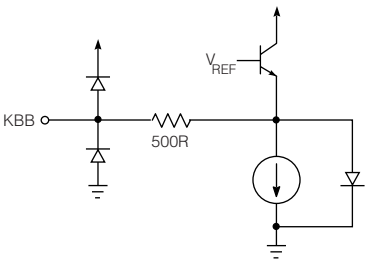


Figure 3-6: KBB

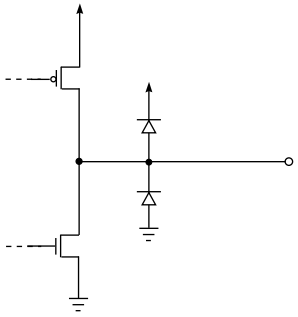


Figure 3-7: Indicator Outputs: SD/$\overline{\text{HD}}$, LOCKED, LOS

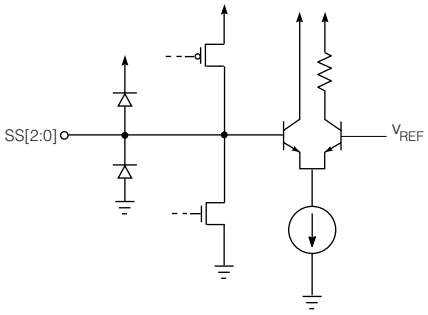


Figure 3-8: Standard Select/Indication Bi-directional Pins

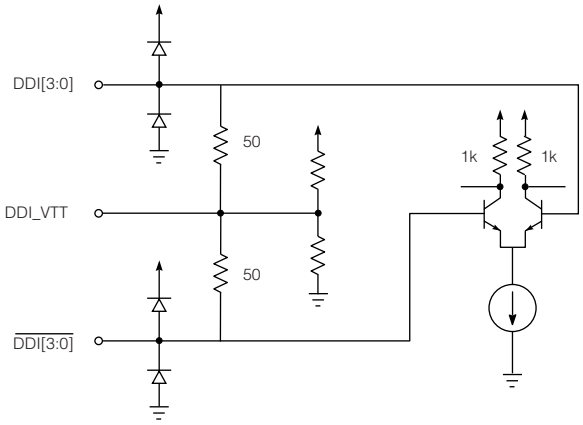


Figure 3-9: Serial Data Inputs

4. Detailed Description

The GS1575A/9075A is a Multi-Rate Serial Digital Reclocker designed to automatically recover the embedded clock from a digital video signal and re-time the incoming video data.

The GS1575A will recover the embedded clock signal and re-time the data from a SMPTE 292M, SMPTE 259M or SMPTE 344M compliant digital video signal.

The GS9075A will recover the embedded clock signal and re-time the data from a SMPTE 259M or SMPTE 344M compliant digital video signal.

Using the functional block diagram (page 2) as a guide, Slew Rate Phase Lock Loop (S-PLL) on page 16 to Output Mute on page 22 describes each aspect of the GS1575A/9075A in detail.

4.1 Slew Rate Phase Lock Loop (S-PLL)

The term “slew” refers to the output phase of the PLL in response to a step change at the input. Linear PLLs have an output phase response characterized by an exponential response whereas an S-PLL’s output is a ramp response (see Figure 4-1). Because of this non-linear response characteristic, traditional small signal analysis is not possible with an S-PLL.

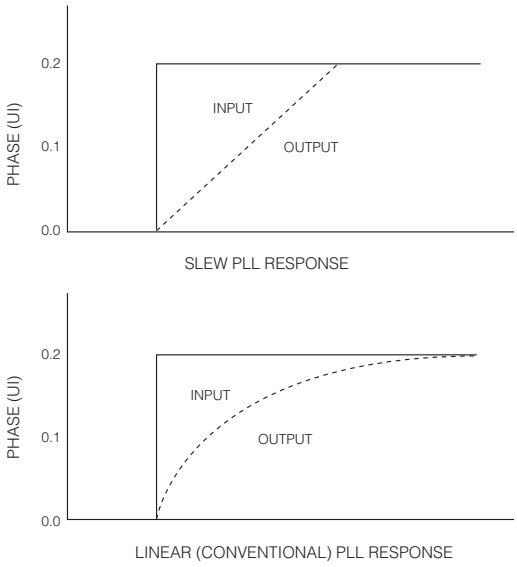


Figure 4-1: PLL Characteristics

The S-PLL offers several advantages over the linear PLL. The Loop Bandwidth of an S-PLL is independent of the transition density of the input data. Pseudo-random data has a transition density of 0.5 verses a pathological signal which has a transition density of 0.05. The loop bandwidth of a linear PLL will change proportionally with this change in transition density. With an S-PLL, the loop bandwidth is defined by the jitter at the data input. This translates to infinite loop bandwidth with a zero jitter input signal. This allows the loop to correct for small variations in the input jitter quickly, resulting in very low output jitter. The loop bandwidth of the GS1575A/9075A's PLL is defined at 0.2UI of input jitter.

The PLL consists of two acquisition loops. First is the Frequency Acquisition (FA) loop. This loop is active when the device is not locked and is used to achieve lock to the supported data rates. Second is the phase acquisition (PA) loop. Once locked, the PA loop tracks the incoming data and makes phased corrections to produce a re-clocked output.

4.2 VCO

The internal VCO of the GS1575A/9075A is a ring oscillator. It is trimmed at the time of manufacture to capture all data rates over temperature and operation voltage ranges.

Integrated into the VCO is a series of programmable dividers used to achieve all serial data rates, as well as additional dividers for the frequency acquisition loop.

4.3 Charge Pump

A common charge pump is used for the PLL of the GS1575A/9075A.

During frequency acquisition, the charge pump has two states, "pump-up" and "pump-down," which is produced by a leading or lagging phase difference between the input and the VCO frequency.

During phase acquisition, there are two levels of "pump-up" and two levels of "pump down" produced for leading and lagging phase difference between the input and VCO frequency. This is to allow for greater precision of VCO control.

The charge pump produces these signals by holding the integrated frequency information on the external loop-filter capacitor, C_{LF}. The instantaneous frequency information is the result of the current flowing through an internal resistor connected to the loop-filter capacitor.

4.4 Frequency Acquisition Loop — The Phase-Frequency Detector

An external crystal of 14.140 MHz is used as a reference to keep the VCO centered at the last known data rate. This allows the device to achieve a fast synchronous lock, especially in cases where a known data rate is interrupted. The crystal reference is also used to clock internal timers and counters. To keep the optimal performance of the reclocker over all operating conditions, the crystal frequency must be 14.140 MHz, +/-50ppm. The GO1535 meets this specification and is available from GENNUM.

The VCO is divided by a selected ratio which is dependant on the input data rate. The resultant is then compared to the crystal frequency. If the divided VCO frequency and the crystal frequency are within 1% of each other, the PLL is considered to be locked to the input data rate.

4.5 Phase Acquisition Loop — The Phase Detector

The phase detector is a digital quadrature phase detector. It indicates whether the input data is leading or lagging with respect to a clock that is in phase with the VCO (I-clk) and a quadrature clock (Q-clk). When the phase acquisition loop (PA loop) is locked, the input data transition is aligned to the falling edge of I-clk and the output data is re-timed on the rising edge of I-clk. During high input jitter conditions (>0.25UI), Q-clk will sample a different value than I-clk. In this condition, two extra phase correction signals will be generated which instructs the charge pump to create larger frequency corrections for the VCO.

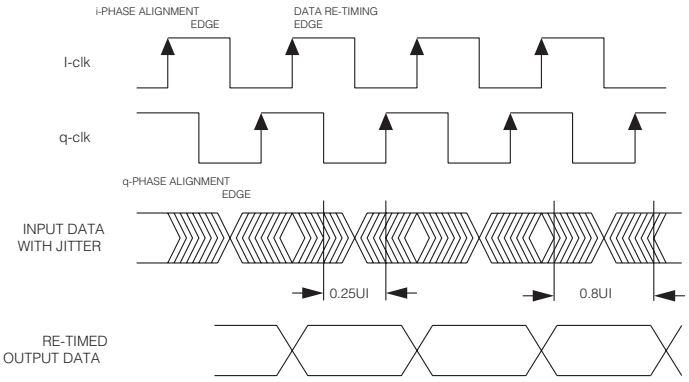


Figure 4-2: Phase Detector Characteristics

When the PA loop is active, the crystal frequency and the incoming data rate are compared. If the resultant is more that 2%, the PLL is considered to be unlocked and the system jumps to the FA loop.

4.6 4:1 Input Mux

The 4:1 input mux allows the connection of four independent streams of video/data. There are four differential inputs (DDI[3:0] and $\overline{\text{DDI}}$[3:0]). The active channel can be selected via the DDI_SEL[1:0] pins. Table 4-1 shows the input selected for a given state at DDI_SEL[1:0].

Table 4-1: Bit Pattern for Input Select

DDI_SEL[1:0]	Selected Input
00	DDI0
01	DDI1
10	DDI2
11	DDI3

The DDI inputs are designed to be DC interfaced with the output of the GS1524A/9064A Cable Equalizer. There are on chip 50Ω termination resistors which come to a common point at the DDI_VT pins. Connect a 10nF capacitor to this pin and connect the other end of the capacitor to ground. This terminates the transmission line at the inputs for optimum performance.

If only one input pair is used, connect the unused positive inputs to +3.3V and leave the unused negative inputs floating. This helps to eliminate crosstalk from potential noise that would couple to the unused input pair.

4.7 Automatic and Manual Data Rate Selection

The GS1575A/9075A can be configured to manually lock to a specific data rate or automatically search for and lock to the incoming data rate. The AUTO/$\overline{\text{MAN}}$ pin selects automatic data rate detection mode (Auto mode) when HIGH and manual data rate selection mode (Manual mode) when LOW.

In Auto mode, the SS[2:0] bi-directional pins become outputs and the bit pattern indicates the data rate that the PLL is locked to (or previously locked to). The "search algorithm" cycles through the data rates and starts over if that data rate is not found (see Figure 4-3).

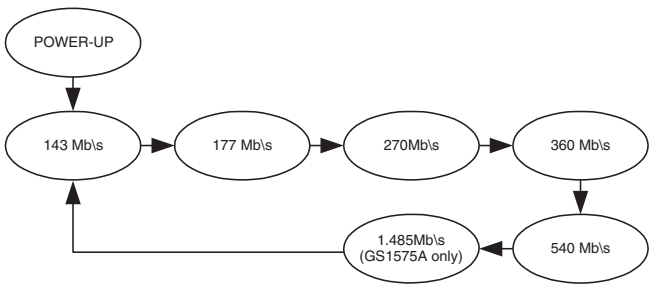


Figure 4-3: Data Rate Search Pattern

In Manual mode, the SS[2:0] pins become inputs and the data rate can be programmed by the application layer. In this mode, the search algorithm is disabled and the PLL will only lock to the data rate selected.

Table 4-2 shows the SS[2:0] pin settings for either the data rate selected (in Manual mode) or the data rate that the PLL has locked to (in Auto mode).

Table 4-2: Data Rate Indication/Selection Bit Pattern

SS[2:0]	Data Rate (Mb/s)
000	143
001	177
010	270
011	360
100	540
101*	1485/1483.5

* This setting only applies to the GS1575A. For the GS9075A, when AUTO/$\overline{\text{MAN}}$ is LOW, the pin settings SS[0:2] = 101 will be ignored by the device.

NOTE: When in Auto mode the device may be susceptible to becoming ‘stuck’ when attempting to acquire lock to signal. When in the ‘stuck’ mode the GS1575A/9075A will not lock to any frequency and the data rate indication pins (SS[2:0]) will indicate the 143Mb/s rate and that the lock detect pin (LOCKED) is in a LOW logic state. This fault may occur when powering up, when searching for a SMTPE data rate, and when changing from one data rate to another. The following workaround need only be used when a ‘stuck’ condition is detected. If operating in Automatic Data Rate Select Mode (AUTO/MANb = ‘1’):

1. Switch to Manual Data Rate Select Mode (AUTO/MANb = ‘0’).
2. Force a data rate other than 143Mb/s on the SS[2:0] pins.
3. Switch back into Automatic Data Rate Select Mode (AUTO/MANb = ‘1’).

4.8 Bypass Mode

In Bypass mode, the GS1575A/9075A passes the data at the inputs directly to the outputs. There are two pins that control the bypass function: BYPASS and AUTOBYPASS.

When BYPASS is set HIGH by the application layer, the GS1575A/9075A will be in Bypass mode.

When AUTOBYPASS is set HIGH by the application layer, the GS1575A/9075A will be configured to enter Bypass mode only when the PLL has not locked to a data rate. When BYPASS is set HIGH, AUTOBYPASS will be ignored.

When the PLL is not locked, and both BYPASS and AUTOBYPASS are set LOW, the serial digital output DDO/$\overline{\text{DDO}}$ will produce invalid data.

4.9 DVB-ASI Operation

The GS1575A/9075A will also re-clock DVB-ASI at 270 Mb/s. When reclocking DVB-ASI data set the ASI/$\overline{177}$ pin HIGH to prevent a false lock to 177Mb/s. If ASI/$\overline{177}$ is not set HIGH, a false lock may occur since there is a harmonic present in idle patterns (K28.5) which is very close the 177 Mb/s data rate (EIC 1179). Note that setting the ASI/$\overline{177}$ pin HIGH will disable the 177 Mb/s search when the device is in Auto mode, consequently the GS1575A/9075A will not lock to that data rate.

4.10 Lock and LOS Indicators

The LOCKED signal is an active high output which indicates when the PLL is locked.

The internal lock logic of the GS1575A/9075A includes a system which monitors the Frequency Acquisition Loop and the Phase Acquisition Loop as well as a monitor to detect harmonic lock.

The LOS (Loss of Signal) output is an active HIGH output which indicates the absence of data transitions at the DDIx input. In order for this output to be asserted, transitions must not be present for a period of typically 5.14 us. After this output has been asserted, LOS will deassert typically 5.14 us after the appearance of a transition at the DDIx input. This timing relationship is shown in Figure 4-4:

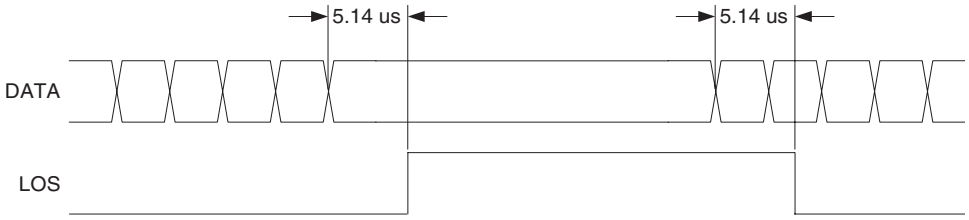


Figure 4-4: LOS signal timing

NOTE: LOS is sensitive to transitions appearing at the input, and does not distinguish between transitions caused by input data, and transitions due to noise.

4.11 Output Drivers and Serial Clock Outputs

The device's serial digital data outputs (DDO/$\overline{\text{DDO}}$) have a nominal voltage of 800mv single ended or 1600mV differential when terminated into a 50Ω load.

The GS1575A/9075A may also be configured to output a serial clock at the data output rate. The internal serial clock output block is powered via the SCO_ENABLE pin. When SCO_ENABLE is connected to VCC, a differential serial clock output will be present on SCO/$\overline{\text{SCO}}$. Otherwise, when SCO_ENABLE is connected to GND, the clock output block will be powered down and the device will have reduced power consumption.

NOTE: The SCO_ENABLE signal should have a 1.5mA drive strength to maintain a supply voltage of 3.3 +/- 0.165V.

Clock and data alignment is shown in Figure 4-5.

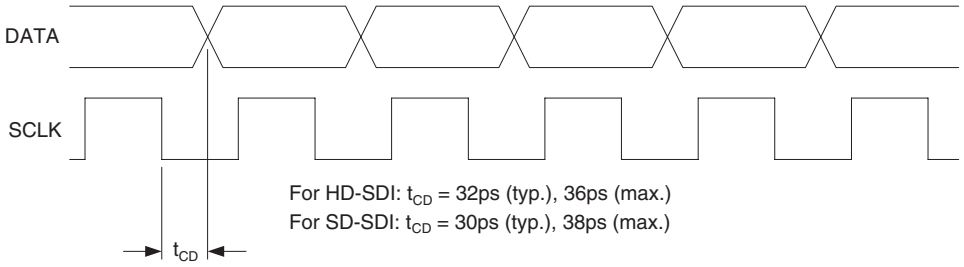


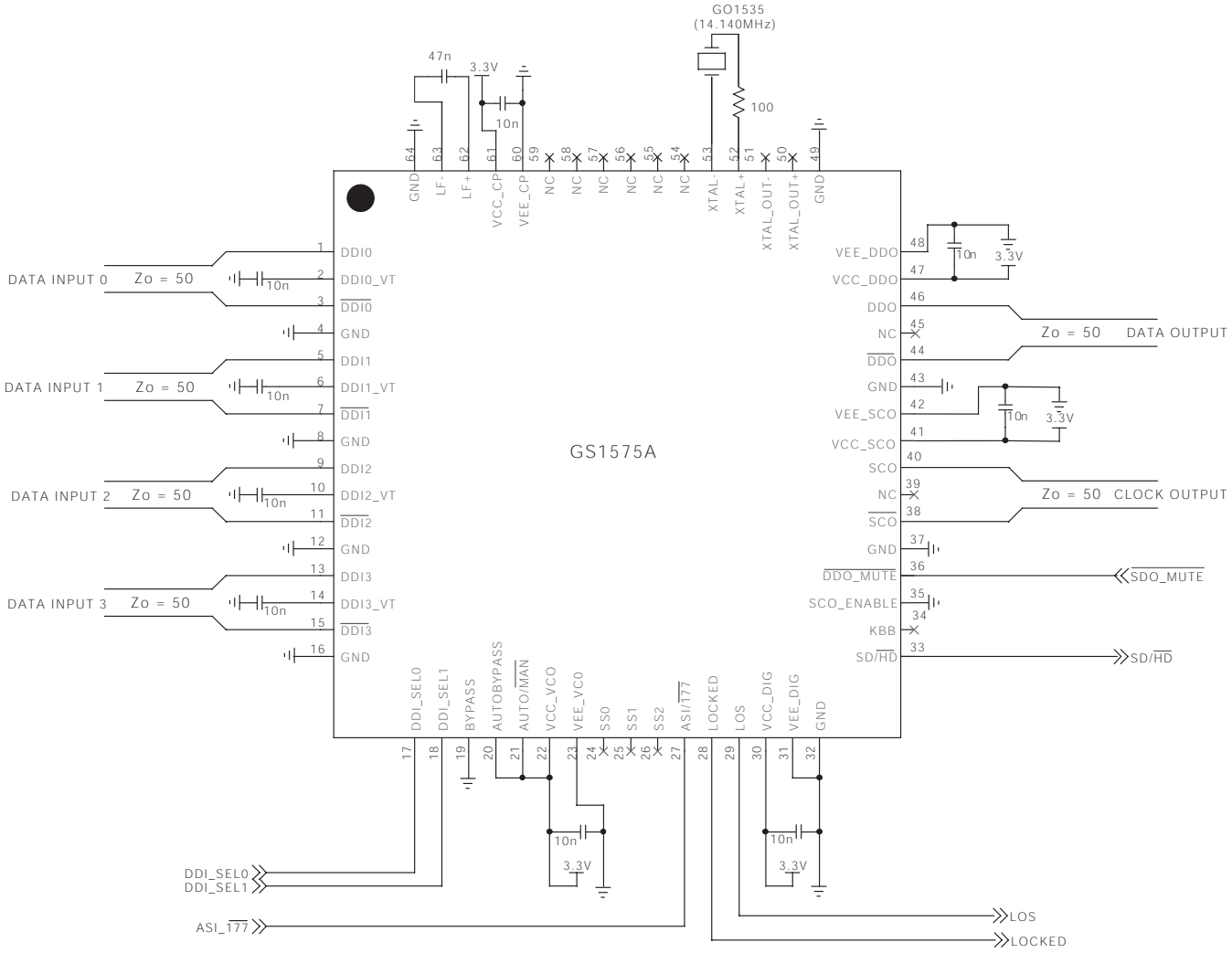
Figure 4-5: Clock and Data Alignment

4.12 Output Mute

The $\overline{\text{DDO\_MUTE}}$ pin is provided to allow muting of the re-timed output.

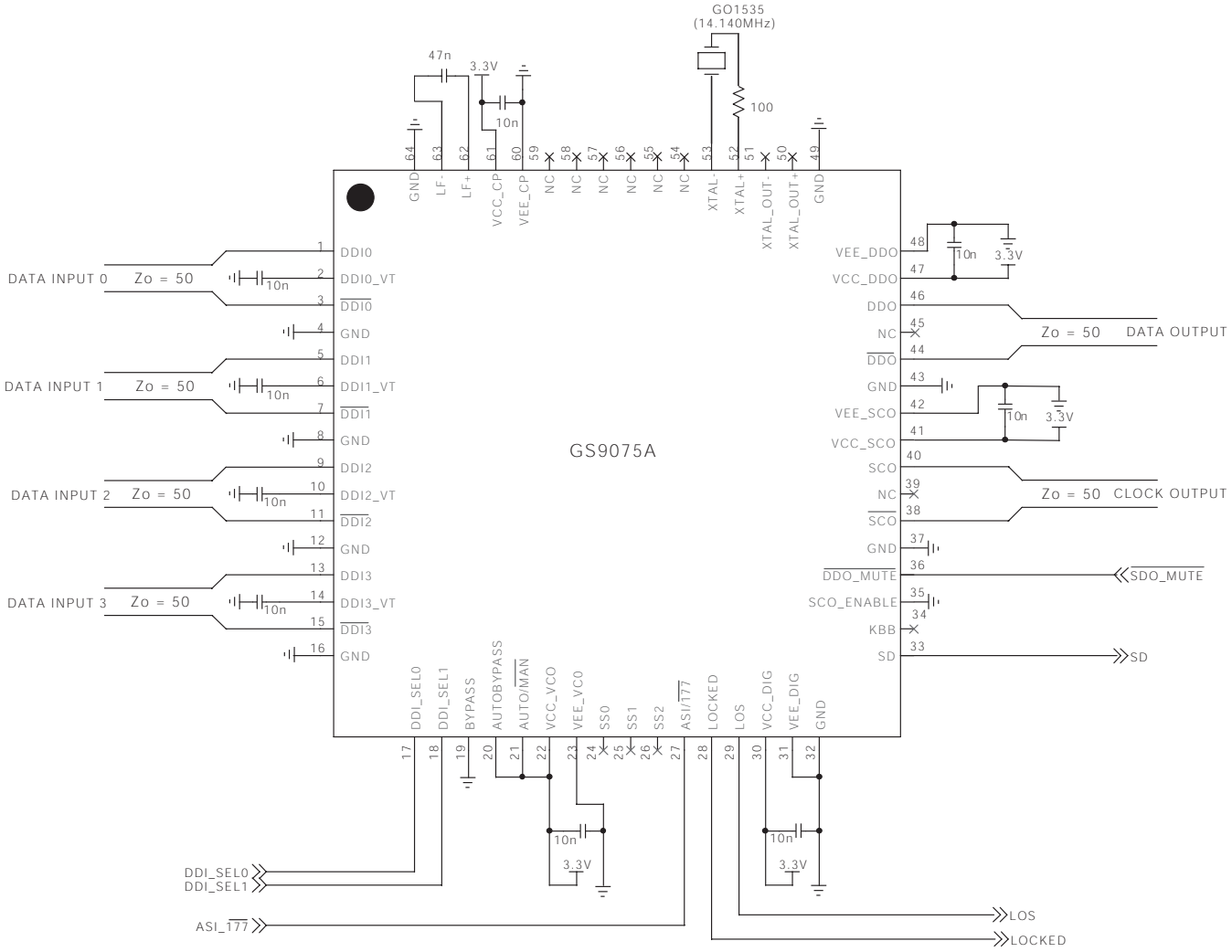
When the PLL is locked and the device is reclocking, setting $\overline{\text{DDO\_MUTE}}$ = LOW will force the serial digital outputs DDO/$\overline{\text{DDO}}$ to mute. However, if the GS1575A/9075A is in Bypass mode, (AUTOBYPASS = HIGH and/or BYPASS = HIGH), $\overline{\text{DDO\_MUTE}}$ will have no effect on the output.

5. Typical Application Circuits



Note: All resistors in ohms and all capacitors in Farads.

Figure 5-1: GS1575A Typical Application Circuit

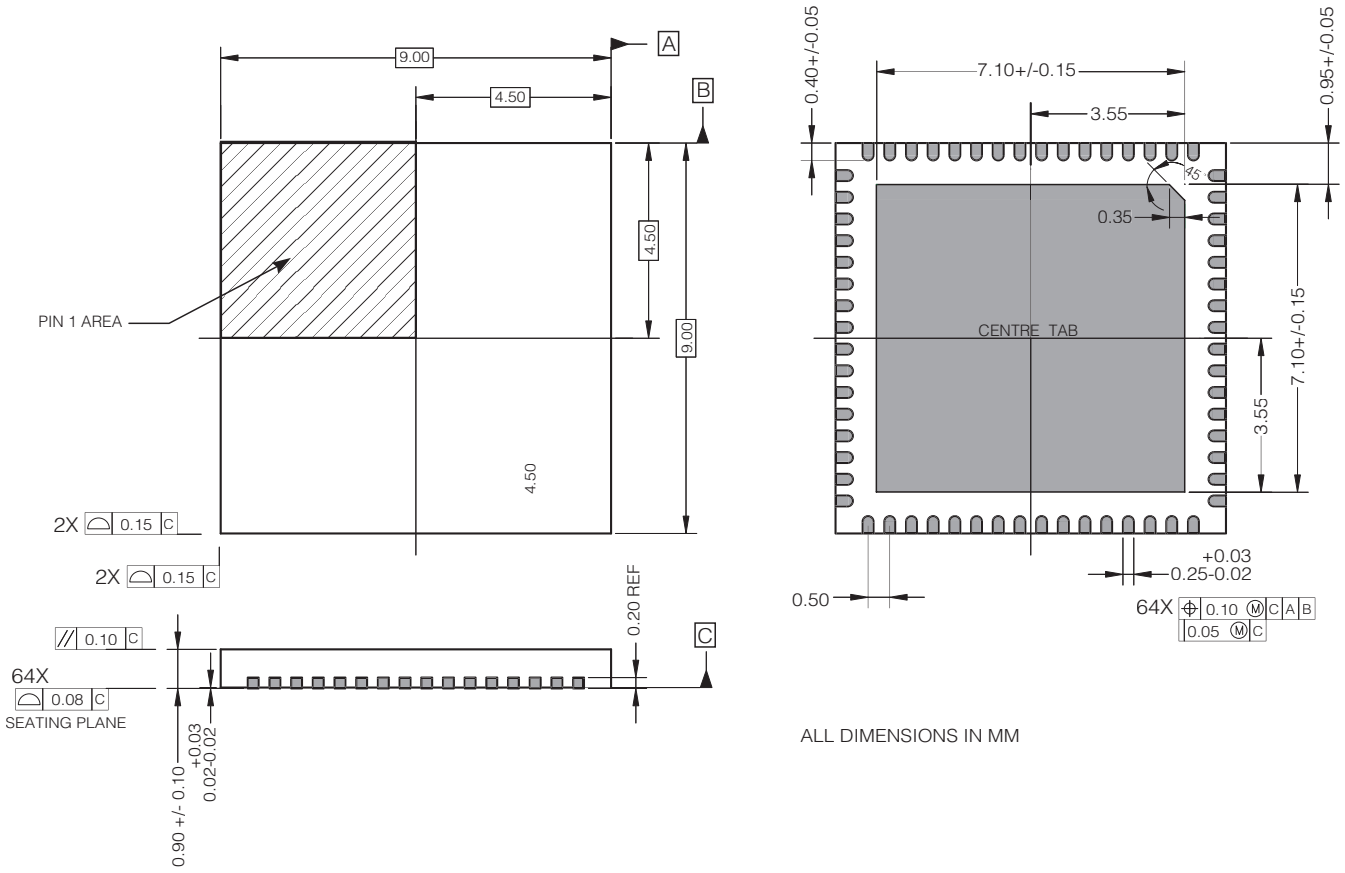


Note: All resistors in ohms and all capacitors in Farads.

Figure 5-2: GS9075A Typical Application Circuit

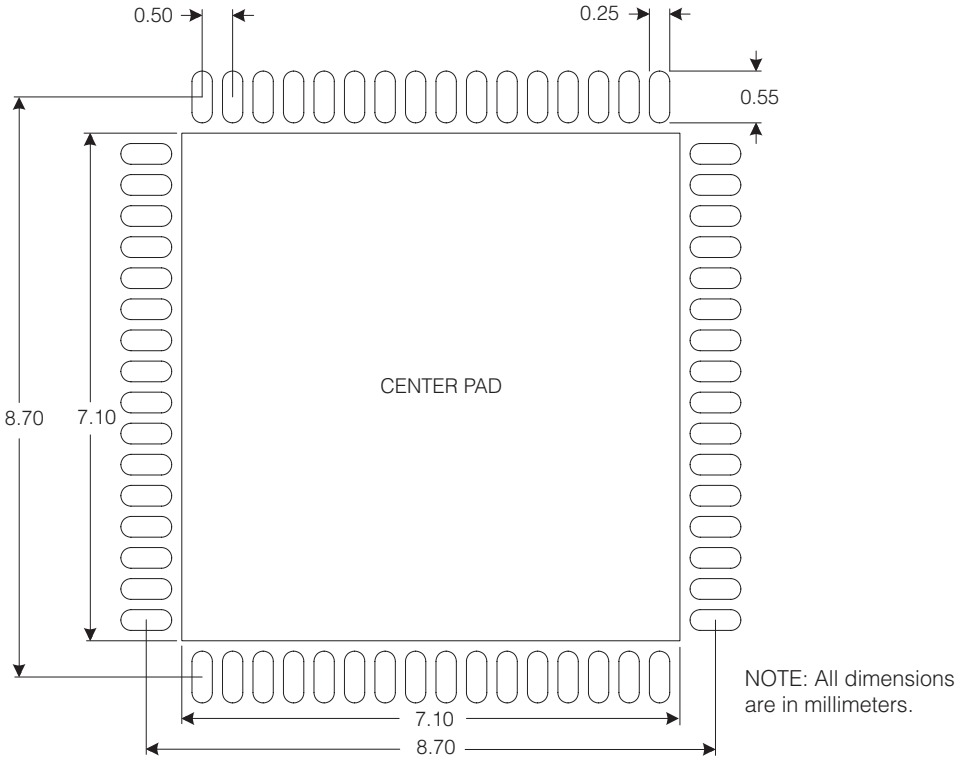
6. Package & Ordering Information

6.1 Package Dimensions



ALL DIMENSIONS IN MM

6.2 Recommended PCB Footprint



The center pad of the PCB footprint should be connected to the ground plane by a minimum of 36 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	9mm x 9mm 64-pin QFN
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	9.1°C/W
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	21.5°C/W
Psi, Ψ	0.2°C/W
Pb-free and RoHS Compliant	Yes

6.4 Ordering Information

	Part Number	Package	Temperature Range
GS1575A	GS1575ACNE3	Pb-free 64-pin QFN	0°C to 70°C
GS9075A	GS9075ACNE3	Pb-free 64-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
A	136456	–	April 2005	New Document.
0	137416	–	December 2005	Converted to Data Sheet. Added block diagram, pinout, DC and AC electrical, and circuit information for serial clock output support. Added information on GS9075A. Added LOS support information. Corrected minor typing errors. Corrected maximum Serial Digital Output swing to 2200 mV. Corrected packaging diagram.
1	140616	39754	June 2006	Added note on 143Mb/s lock issue in section 4.7 Automatic and Manual Data Rate Selection.

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